

INDIAN INSTITUTE OF TECHNOLOGY BOMBAY

MATERIALS MANAGEMENT DIVISION

Powai, Mumbai - 400076

<u>Technical Specification :</u> <u>Switch Matrix System</u>

Index	Description	Specification (to be matched or exceeded)
1	List of atleast 5 international semiconductor industrial customers	
2	List 5 international academic/lab customers (at least 10)	
3	List Indian customers (note repeat purchases if any)	
4	Mainframe with Available Card Slot which can be expanded from 1-6 in units of 1 to share input and expand output ports	6
5	IEEE-488	IEEE-488.1 compliant.
6	USB 2.0 Device (rear panel type B)	Full and high speed, USBTMC compliant.
7	Digital I/O Interface	
8	Connector	22-pin female D.
9	Input/Output Pins	10 open drain I/O bits.
10	Absolute Maximum Input Voltage	5V.
11	Absolute Minimum Input Voltage	-0.2V.
12	Maximum Source Current (flowing out of Digital I/O bit)	900µA.
13	Maximum Sink Current @ Maximum Logic Low Voltage (0.7V)	-4.5mA.
14	Absolute Maximum Sink Current (flowing into Digital I/O pin)	–10mA. 5V
15	Power Supply Pin	Limited to 600mA, solid state fuse protected.

16	Ethernet	RJ-45 connector, 10/100BaseT, Auto- MDIX.
17	LXI Compliance	LXI Version 1.2.
18	Power Supply	100V to 240VAC, 50Hz–60Hz, 210VA max.
19	Relay Drive	30W (6V at 5.0A) max. per slot, 162W (6V at 27A) max. for all slots.
20	Max Dimensions with Card Installed	400mm high × 432mm wide × 700mm deep
21	Max Weight	15kg
22	Card Description	8×12 Low-Current, High-Speed Matrix Card, with 3-lug Triax Row and Column connects
23	channel.close ('ch_list') or channel.open ('ch_list') Single Command Execution Time (ms)	1.9
24	TRIGGER RESPONSE TIME Maximum Trigger Rate (setups per second)1	≥815.
25	Trigger in to start of Matrix Ready Pulse (DDC Mode)	≤85µs.
26	Trigger in to trigger out	≤0.5µs.
27	Trigger Timer accuracy	≤0.5µs.
28	High-Speed Card	Need 3 Nos of each; Card Specs below
29	MATRIX CONFIGURATION	Single 8 rows×12 columns. Expanding the columns can be done internally by connecting the rows of multiple cards together with coax jumpers.
30	CROSS POINT CONFIGURATION	2-pole Form A (Signal Guard).
31	CONNECTOR TYPE	3-lug triax (Signal, Guard, Chassis).
32	MAXIMUM SIGNAL LEVEL (Pin-to-pin or Pin-to-Chassis)	200V. 2A carry current.
33	CONTACT LIFE Cold Switching	10^8 closures.
34	OFFSET CURRENT	100fA max., 10fA typical (with 0V applied to inputs and outputs).
35	ISOLATION	
36	Path (Signal to Signal)	>10^14 Ohm, 1pF.
37	Common (Signal to Chassis)	>10^14Ohm, <10pF.

38	Settling Time	<2.5s to 400fA (all pathways) after 10V applied(typical).
39	CROSS TALK (1MHz, 50Ohm Load)	<-70dB.
40	INSERTION LOSS (1MHz, 50Ohm Load)	<–0.2dB typical.
41	3dB BANDWIDTH (50ohm Load, 50Ohm Source)	30MHz typical.
42	3dB BANDWIDTH (1MOhm Load, 50Ohm Source)	40MHz typical.
43	RELAY SETTLING TIME	<2ms.
44	ENVIRONMENTAL DETAILS	
44 45	ENVIRONMENTAL DETAILS Operating	0° to 50°C,
44 45 46	ENVIRONMENTAL DETAILS Operating MAXIMUM LEAKAGE	0° to 50°C,
44 45 46 47	ENVIRONMENTAL DETAILS Operating MAXIMUM LEAKAGE Pin to Ground	0° to 50°C, 0.02pA/V.
44 45 46 47 48	ENVIRONMENTAL DETAILS Operating MAXIMUM LEAKAGE Pin to Ground Pin to Pin	0° to 50°C, 0.02pA/V. 0.01pA/V.
44 45 46 47 48 49	ENVIRONMENTAL DETAILS Operating MAXIMUM LEAKAGE Pin to Ground Pin to Pin INSULATION RESISTANCE	0° to 50°C, 0.02pA/V. 0.01pA/V. 10^12 Ohm minimum.
44 45 46 47 48 49 50	ENVIRONMENTAL DETAILS Operating MAXIMUM LEAKAGE Pin to Ground Pin to Pin INSULATION RESISTANCE CAPACITANCE	0° to 50°C, 0.02pA/V. 0.01pA/V. 10^12 Ohm minimum. (Guard Driven)
44 45 46 47 48 49 50 51	ENVIRONMENTAL DETAILS Operating MAXIMUM LEAKAGE Pin to Ground Pin to Pin INSULATION RESISTANCE CAPACITANCE Path to Path	0° to 50°C, 0.02pA/V. 0.01pA/V. 10^12 Ohm minimum. (Guard Driven) 2pF typical.